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10/521,054	01/12/2005	Takashi Yokokawa	09812.0200	6969

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/521,054	YOKOKAWA ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-41 have been submitted for examination
- Claims 1-41 have been rejected

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

2. Figures (1-14) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 41 rejected under 35 U.S.C. 101 because the claim invention is directed to non-statutory subject matter. Each limitation in claim 41 comprises an abstract algorithm that can be carried by hand or computer software program element and

is **not tangibly embodied**. Abstract algorithms are non-statutory. **Un-executed** Computer programs are non-statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 6 should read:

". .....when the sub-matrices whose weight is 2 or more from among the sub matrices representing said check matrix are represented in the form of the sum of the unit matrix, ~~**whose weight is 1**~~, the quasi-unit matrix, or the shift matrix **whose weight is 1**.

Appropriate action is required.

5. Claim 20 should read:

"The decoding apparatus according to claim18, wherein said first decoding in-progress results stored at the same address in each of said two single-port RAMs"

Appropriate action is required.

6. Claim 34 is rejected for the same reasons as per claim 20.

Appropriate action is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Richardson et al. US patent no. 6633856 (Hereinafter Richardson).

8. In regard to claim 1, Richardson teaches:

- A decoding apparatus for decoding LDPC (Low Density Parity Check) codes, when using as a sub-matrix, a (P x P) unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said shift matrix, or a (P X P) 0-matrix, a check matrix of said LDPC codes is represented by a combination of a plurality of said sub-matrices, said decoding apparatus comprising:
- first computation means for simultaneously performing P check node computations for decoding said LDPC codes; and

(Note: Figure 16, reference sign (1609) in Richardson. The Examiner notes that check node is being referred to as constraint node in Richardson).

(Note: Col. 11, lines (13-15) in Richardson)

- second computation means for simultaneously performing P variable node computations for decoding said LDPC codes.

(Note: Figure 16, reference sign (1608) in Richardson)

(Note: Col. 11, lines (13-15) in Richardson)

9. In regard to claim 2, Richardson teaches:

- The decoding apparatus according to Claim 1, wherein said first computation means has P check node calculators for performing check node computations, and said second computation means has P variable node calculators for performing variable node computations.

(Note: Col.23, lines (35-45) in Richardson)

10. In regard to claim 3, Richardson teaches:

- The decoding apparatus according to Claim 1, further comprising:
- message storage means for simultaneously reading and writing message data corresponding to P edges, which is obtained as a result of said P check node computations or said P variable node computations.

(Note: Figure 9, reference sign (906) and col. 21, lines (44-47) in Richardson)

11. In regard to claim 4, Richardson teaches:

- The decoding apparatus according to Claim 3, wherein said message storage means stores message data corresponding to the edges,

which are read during the check node computation in such a manner that 1s of the check matrix are packed closer in the row direction.

(Note: Col. 21, lines (39-65) in Richardson)

12. In regard to claim 5, Richardson teaches:

- The decoding apparatus according to Claim 3, wherein said message storage means stores message data corresponding to edges, which are read during the variable node computation in such a manner that 1s of the check matrix are packed closer in the column direction.

(Note: Figure 8, sing (806) and col.15, lines (52-65) in Richardson)

13. In regard to claim 6, Richardson teaches;

- The decoding apparatus according to Claim 3, wherein said message storage means stores, at the same address, messages corresponding to P edges belonging to a unit matrix whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix.

(Note; col. 22, lines (35-40) in Richardson)

14. In regard to claim 7, Richardson teaches:

- The decoding apparatus according to Claim 3, wherein said message storage means comprises number-of-rows/p columns/p FIFOs and number-of-columns/p FIFOs and

- said number-of-rows/p columns/p FIFOs and said number-of-columns/p FIFOs each have a number of words corresponding to the weight of the row and the weight of the column of said check matrix, respectively.

(Note: col. 20, line 44 in Richardson)

15. In regard to claim 8, Richardson teaches:

- The decoding apparatus according to Claim 3, wherein said message storage means comprises a RAM (Random Access Memory, and said RAM stores said message data in the read-out sequence such a manner as to be packed closer and reads said message data in the storage position sequence.

(Note: Figure 15, reference sign (1506) and col. 23, lines (8-10) in Richardson)

16. In regard to claim 9, Richardson teaches:

- The decoding apparatus according to Claim 1, further comprising:
- received information storage means for storing received information of LDPC codes and for simultaneously reading P pieces of said received information.

(Note: col. 21, lines (41-43) In Richardson)

17. In regard to claim 10, Richardson teaches:

- The decoding apparatus according to Claim 9, wherein said received information storage means stores said received information in such a

manner that the received information can be read in the sequence necessary for said variable node computation.

(Note: Figure 15, reference sign (1504) in Richardson)

18. In regard to claim 11, Richardson teaches:

- The decoding apparatus according to Claim 1 further comprising:
- rearranging means for rearranging messages obtained as a result of said P check node computations or said P variable node computations.

(Note: Figure 9, reference character (904), col. 16, lines (50-60), Figure 15, reference sign (1504) and col. 22, lines (40-60) in Richardson)

19. In regard to claim 12, Richardson teaches:

- The decoding apparatus according to Claim 11, wherein said rearranging means comprises a barrel shifter.

(Note: col.21, lines (52-65) in Richardson)

20. In regard to claim 13, Richardson teaches:

- The decoding apparatus according to Claim 1, wherein said first computation means and said second computation means determine messages corresponding to P edges.

(Note: Figure 15 in Richardson)

21. In regard to claim 14, Richardson teaches:

- The decoding apparatus according to Claim 1, wherein said first computation means performs some of said P check node computations and said P variable node computations, and said second computation

means performs some of the others of said P variable node computations.

(Note: Figure 16 and col. 24, lines (30-65) in Richardson)

22. In regard to claim 15, Richardson teaches:

- The decoding apparatus according to Claim 14, wherein said first computation means comprises P calculators for performing some of said P check node computations and said P variable node computations, and said second computation means comprises P calculators for performing some of the others of said P variable node computations.

(Note: Figure 16 and col. 24, lines (30-65) in Richardson)

23. In regard to claim 16, Richardson teaches:

- The decoding apparatus according to Claim 14, further comprising:
- first decoding in-progress result storage means for simultaneously reading and writing first decoding in-progress results corresponding to P edges, which are obtained by said first computation means by performing some of said P check node computations and said P variable node computations.

(Note: Figure 15, reference sign (1506) in Richardson)

24. In regard to claim 17, Richardson teaches:

- The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means stores said first decoding

in-progress results corresponding to the edge, which are read when some of the others of said P variable node computations are performed, in such a manner that 1s of the check matrix are packed closer in the row direction.

(Note: Col. 21, lines (39-65) in Richardson)

25. In regard to claim 18, Richardson teaches:

- The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means are two single-port RAMs (Random Access Memories).

(Note: Figure 17, reference signs (1706) and (1707) in Richardson)

26. In regard to claim 19, Richardson teaches:

- The decoding apparatus according to Claim 18, wherein said two single-port RAMS alternately store said first decoding in-progress results in units of said first decoding in-progress results corresponding to edges of P rows of said check matrix.

(Note: col. 26, lines (25-45) in Richardson)

27. In regard to claim 20, Richardson teaches:

- The decoding apparatus according to Claim 18, wherein said two single-port RAMs (Random Access Memories) each read said first decoding in-progress results stored at the same address.

(Note: col. 26, lines (25-45) in Richardson)

28. In regard to claim 21, Richardson teaches:

- The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means stores, at the same address, said first decoding in-progress results corresponding to P edges belonging to a unit matrix whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix.

29. In regard to claim 22, Richardson teaches:

- The decoding apparatus according to Claim 14, further comprising:
- second decoding in-progress result storage means for simultaneously reading and writing said second decoding in-progress results corresponding to P edges, which are obtained by said second computation means by performing some of the others of said P variable node computations.

(Note: Col. 21, lines (39-65) in Richardson)

30. In regard to claim 23, Richardson teaches:

- The decoding comprising:
- apparatus according to Claim 14, further received information storage means for storing information of LDPC codes and simultaneously reading pieces of received information.

(Note: Figure 15, reference design (1518) in Richardson)

31. In regard to claim 24, Richardson teaches:

- The decoding apparatus according to Claim 23, wherein said received information storage means stores said received information in such a manner that said received information can be read in the sequence necessary for some of the others of said P variable node computations.

(Note: Figure 15, reference sign (1504) and col. 22, lines (41-55) in Richardson)

32. In regard to claim 25, Richardson teaches:

- The decoding apparatus according to Claim 14, further comprising:
- rearranging means for rearranging first decoding in-progress results obtained by said first computation means by performing some of said P check node computations and said P variable node computations, or second decoding in-progress results obtained by said second computation means by performing some of the others of said P variable node computations.

(Note: Figure 15, reference sign (1504) and col. 22, lines (41-55) in Richardson)

33. In regard to claim 26, Richardson teaches:

- The decoding apparatus according to Claim 25, wherein said rearranging means comprises a barrel shifter.

(Note: col. 22, line 45 in Richardson)

34. In regard to claim 27, Richardson teaches:

- The decoding apparatus according to Claim 1, wherein said first computation means performs some of said P check node computations, and
- said second computation means performs some of the others of said P check node computations, and said P variable node computations.

(Note: Figure 16 and col. 24, lines (30-65) in Richardson)

35. In regard to claim 28, Richardson teaches:

- The decoding apparatus according to Claim 27, wherein
- said first computation means comprises P calculators for performing some of said P check node computations, and
- said second computation means comprises P calculators for performing some of the others of said P check node computations, and said P variable node computations.

(Note: Col.23, lines (35-45) in Richardson)

36. In regard to claim 29, Richardson teaches:

- The decoding apparatus according to Claim 27, further comprising:
- first decoding in-progress result storage means for simultaneously reading and writing first decoding in-progress results corresponding to P edges, which are obtained by said first computation means by performing some of said P check node computations.

(Note: Figure 15, reference sign (1506) in Richardson)

37. Claim 30 is rejected for the same reasons as per claim 22.

38. Claim 31 is rejected for the same reasons as per claim 5.

39. Claim 32 is rejected for the same reasons as per claim 18.

40. Claim 33 is rejected for the same reasons as per claim 19.

41. Claim 34 is rejected for the same reasons as per claim 20.

42. In regard to claim 35, Richardson teaches:

- The decoding apparatus according to Claim 30, wherein
- said second decoding in-progress result storage means stores, at the same address, said second decoding in-progress results corresponding to P edges belonging to a unit whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix.

(Note: Figure 11, reference character (1102) in Richardson)

43. Claim 36 is rejected for the same reasons as per claim 9.

44. Claim 37 is rejected for the same reasons as per claim 10.

45. Claim 38 is rejected for the same reasons as per claim 11.

46. Claim 39 is rejected for the same reasons as per claim 12.

47. In regard to claim 40, Richardson teaches:

- A decoding method for use with a decoding apparatus for decoding LDPC (Low Density Parity Check) codes, when using as a sub-matrix,

a (P x P) unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said shift matrix, or a (P x P) 0-matrix, a check matrix of LDPC codes is represented by a combination of a plurality of said sub- matrices, said decoding method comprising:

- a first computation step of simultaneously performing P check node computations for decoding said LDPC codes; and

(Note: Figure 16, reference sign (1609) in Richardson. The Examiner notes that check node is being referred to as constraint node in Richardson).

(Note: Col. 11, lines (13-15) in Richardson)

- a second computation step of simultaneously performing P variable node computations for decoding said LDPC codes.

(Note: Figure 16, reference sign (1608) in Richardson)

(Note: Col. 11, lines (13-15) in Richardson)

(Note: Claim 31 in Richardson)

48. Claim 41 is rejected for the same reasons as per claim 40.

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Jin et al. US patent no. 6961888 teaches method and apparatus for encoding LDPC codes.
- Richardson et al. US publication no. US 2005/0278606 teaches method and apparatus for decoding LDPC codes.
- Richardson US patent no. teaches method and apparatus for performing LDPC code operations using a multi-level permutation.
- Richardson US publication no. 2004/0187129 teaches method and apparatus for performing LDPC code operations using a multi-level permutation.
- Richardson et al. US patent no. 6938196 teaches node processors for use in party check decoders.
- Hocevar US publication no. US 2004/0034828 teaches Hardware efficient low density parity check code for digital communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

4/1/06

GUY LAMARRE
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